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EXAMINER	
PATEL, NIRAV B	
ART UNIT	PAPER NUMBER
2135	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,678	BAJIKAR ET AL.	
	Examiner	Art Unit	
	Nirav Patel	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2007 (Amendment)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/27/07 (6)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on June 26, 2007 has been entered. Claims 1-27 are pending. Claims 1, 7, 10 are amended and Claims 23-27are newly added by the applicant.

2. The Office would like to notify the Applicant that there has been a change in the Examiner to conduct the future examination and prosecution processes of the currently pending application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-17, 23, 24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Poisner et al (US Patent No. 7,076,669).

As per claim 1, Poisner discloses:

a chipset; a bus coupled to the chipset to communicate a trusted data cycle to an internal component of the computer system [Fig. 1, col. 2 lines 56-59, col. 3 lines 6-51];

and a circuit coupled to the bus to scan for the trusted data cycle detect the trusted data cycle [Fig. 1, col. 4 lines 26-33], and provide a filtering mechanism to prevent that a device external to the computer system from accessing the trusted data cycle [Fig. 1, col. 5 lines 6-13].

As per claim 2, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the bus is a Low Pin Count bus [Fig. 1, col. 3 line 46].

As per claim 3, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the component provides protected memory storage [Fig. 1].

As per claim 4, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the component provides platform authentication [col. 1 lines 14-20].

As per claim 5, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the component maintains a protected path between the chipset and a keyboard [Fig. 1, col. 5 lines 15-18, col. 7 lines 29-32].

As per claim 6, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the computer system is a notebook computer [Fig. 1, col. 1 line 15].

As per claim 7, Poisner discloses:

means for transmitting data on a Low Pin Count (LPC) bus [Fig. 1, col. 3 line 46]; and filtering means for scanning for trusted data cycles on the Low Pin Count (LPC) bus and preventing the trusted data cycles on the Low Phi Count (LPC) bus from being accessed by an unauthorized component [Fig. 1, col. 4 lines 26-33, col. 5 lines 6-13].

As per claim 8, the rejection of claim 7 is incorporated and Poisner discloses:
means for connecting an external device to a notebook computer [Fig. 1].

As per claim 9, the rejection of claim 7 is incorporated and Poisner discloses:
means for monitoring data cycles on the LPC bus [Fig. 1, col. 4 lines 26-33].

As per claim 10, it encompasses limitations that are similar to limitations of claim 1. Thus, it is rejected with the same rationale applied against claim 1 above.

As per claim 11, the rejection of claim 10 is incorporated and Poisner discloses:
trusted data cycles begin with a "0101" value [col. 8 lines 16-17].

As per claims 12 and 14, the rejection of claim 10 is incorporated and Poisner discloses:
communicating trusted data cycles between the chipset and a first/a second component [Fig. 1].

As per claims 13 and 15, the rejection of claims 12 and 14 are incorporated and Poisner discloses:

the communication between the chipset and the first/the second component is in plaintext format [Fig. 1].

As per claims 16 and 17, the rejection of claim 15 is incorporated and Poisner discloses: the second component maintains a protected path between the chipset and a keyboard, wherein keystroke data is communicated by the chipset to protected memory and trusted applications [Fig. 1].

As per claims 23, 24 and 27, the rejection of claims 1 and 10 are incorporated and Poisner discloses:

wherein the circuit makes a data cycle that is not a trusted data cycle available to the device external to the computer system [col. 4 lines 57-67, col. 5 line 1].

As per claim 26, the rejection of claim 1 is incorporated and Poisner discloses:

wherein the trusted data cycle begins with a predefined trusted data cycle indicator [Fig. 3 or 4].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al [US Patent No. 7,076,669 -- (Poisner '669)] and in view of Poisner [US Pub No. 7,076,669 -- (Poisner '143)].

As per claim 18, the rejection of claim 12 is incorporated and Poisner '143 discloses: wherein the first component protects secret data of the computer system by encrypting the secret data [paragraph 0024 lines 1-2, 0029 lines 3-6].
Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Poisner '143 with Poisner '669, since one would have been motivated to protect data for creating and maintaining a protected operating environment [paragraph 0029 lines 1-3].

As per claim 19, the rejection of claim 12 is incorporated and Poisner '143 discloses: wherein the secret data is decrypted by hardware of the computer system [paragraph 0024 lines 1-2, 0029 lines 3-6].

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al (US Patent No. 7,076,669) and in view of Yanagisawa (US Patent No. 6,519,669).

As per claim 25, the rejection of claim 1 is incorporated and Poisner teaches the circuit blocks the trusted data cycle [Fig. 1, col. 5 lines 9-13].

Yanagisawa teaches the circuit blocks the data cycle from a docking connector [Fig. 1, 2].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Yanagisawa with Poisner, since one would have been motivated to control docking and undocking a peripheral device while a computer system is in operation [Yanagisawa, col. 1 lines 9-11].

6. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al [US Patent No. 7,076,669 -- (Poisner '669)] and in view of Poisner [US Pub No. 7,076,669 -- (Poisner '143)] and in view of Probst [US Patent No. 5,982,899].

As per claim 20, the rejection of claim 18 is incorporated and Probst discloses:

the first component merges data with the computer system's configuration values [Fig. 1, col. 5 lines 18-39].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Probst with Poisner '669 and Poisner '143, since one would have been motivated to verify configuration of a computer system and prevent altering or bypassing the computer system information [Probst, col. 4 lines 62-63].

As per claim 21, the rejection of claim 18 is incorporated and Probst discloses: wherein the first component requests a system identification request [col. 7 lines 13-17, 34-35].

As per claim 22, the rejection of claim 21 is incorporated and Probst discloses: wherein a trusted third party chip verifies the computer system's identification and sends a response to the first component [col. 3 lines 49-59, col. 7 lines 36-63].

Response to Amendment

7. Applicant has amended claims 1, 7, 10 and added claims 23-27, which necessitated new ground of rejection. See rejection above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see form 892).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nirav Patel whose telephone number is 571-272-5936. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on 571-272-3859. The fax and phone numbers for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

NBP
8/30/07

KIM VU
SUPERVISORY PATENT
TECHNOLOGY CE